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Industrial Electrical Engineering and Automation

Model verification and common mode current analysis of grid connected three phase two level converters

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Abstract

In this Master's thesis an in-depth model of a shunt active filter for high frequency analysis is constructed. The purpose is to enable analysis of higher frequency behavior reaching 1MHz. Using the high frequency model, common mode currents can be simulated.

The model is built using high frequency impedance measurements of the internal components in one of Comsys ABs active filters. The measurement is done up to 10MHz and equivalent circuits are constructed to mimic the parasitic components. The impedance is measured over the components and from the component terminal to ground. The model containing the equivalent circuits is made and calibrated to match the device under test.

Using the measured component values and the measured parasitic elements, a simulation model could be designed. Equivalent circuits were used to model the non-idealities in the components and thus their high frequency behavior. An initial model was run and the simulated signals were compared to the lab setup measurements. The component values were tuned to better match the measured frequencies and damping resulting in a final simulation model. The outcome of the thesis is a model that simulates the overall frequency behavior up to 2 MHz. The major oscillations caused by switching IGBTs and how they are extended through the machine can be observed in the simulation. Fast Fourier transform analysis supports the similarities between measurements and simulations where peaks at relevant frequencies are observed. Common mode currents flowing through parasitic couplings can be approximated using the model. Discussions concerning the frequency and damping adjustments are made where areas such as eddy currents and measuring uncertainties are touched upon. A comparison between reality and simulation is done where differences are analysed and discussed.

The thesis provides a model that can be used up to 2MHz where common mode currents can be approximately simulated, therefore the purpose was achieved. It lays a foundation for continued work concerning EMC and high frequency behavior in active filters. Further work to improve upon the model could be simulating non-ideal IGBTs and locating the large damping resistance present in the lab setup. To use the model in deeper analysis the model should be run in different operation states to ensure the performance of the model is satisfactory.

Acknowledgements

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Chapter 1

Introduction

This work is about detailed modelling of a type of power electronic converter used in the power system. The purpose of the converter in an active filter is to compensate for irregularities and the focus of the project is to increase the detail of the system model.

1.1 Background

1.1.1 Shunt active filters

The shunt active filter is a technology used to minimize different types of disturbances in the grid caused by a load. The disturbances can be seen as the presence of transients, harmonics, phase current unbalance and unwanted reactive power in the grid. These are often caused by industrial loads, but can also be caused by offices and commercial buildings etc. By placing a shunt active filter between the grid and the load, an injection of current is added to compensate for the distorted sine wave, see figure 1.1. This is made in a similar fashion as active noise canceling headphones reduces noise, by adding an inverted signal to the original [1].

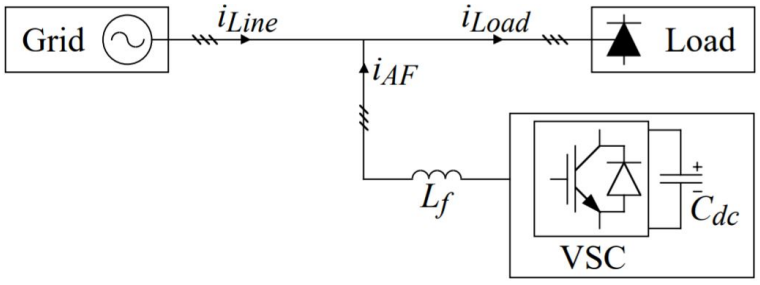


Figure 1.1: Voltage source controlled (VSC) shunt active filter placed between the grid and load. iAF is the injected current.[3, p.15].

1.1.2 EMC

Electromagnetic Interference (EMI) is electromagnetic radiation from devices that pollutes the environment. The damage varies from smaller disturbances that can be neglected to more severe interference that can destroy electric equipment. Electromagnetic compatibility or EMC is the resilience to EMI and the suppression of electromagnetic radiation produced by the electric device itself. The International Electrotechnical Commission defines EMC as "ability of equipment or a system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment" [5]. Generic standards are set for both radiated emissions and cable bound conducted emissions. An example to visualize how electromagnetic incompatibility might take form follows. "*Near the BBC World Service transmitter at Rampisham, Dorset, residents have heard foreign voices through an electric organ and heard the signature tune through a toaster*" [16].

1.2 Challenges

Switching is often used in power electronics converters in order to convert energy between different voltage levels or forms (AC vs DC). Switching however creates unwanted high frequency harmonics that are conducted through parasitic elements in the converter. To avoid interference with other systems in the power grid, these harmonics need to be suppressed. Parasitic elements can be capacitive, inductive and resistive impedances to the chassis and electric ground or between the internal electronics. Through the grounded chassis a circuit-loop is created where the high frequency energy can connect to the ground of the grid, introducing unwanted harmonic currents into the grid. The introduction of such harmonics is in some cases forbidden by regulations and violations may lead to fines.

The goal of this master's thesis project is to build a detailed high frequency model of a shunt active filter. The model's frequency accuracy shall be increased to 1MHz. Using this model the common mode current paths in a grid connected 3 phase 2 level converter can be simulated and analysed. The purpose of building a detailed model is to enable more accurate simulation work to be done on active filters. Furthermore it will give a better understanding of EMC in active filters and how switched electronics affect their immediate surroundings. The results can also improve understanding on a component level.

1.3 Project partners

This Master's thesis has been made in collaboration with the company Comsys AB and the division of Industrial Electrical Engineering and Automation at LTH. The division of Biomedical Engineering has been involved when measuring parasitic components.

1.4 Earlier studies

The model was based on previous LTH and Comsys AB projects of a converter referred to as the "device under test" (DUT). Low frequency (<200kHz) parameters for modelling the converter have been measured previously and were utilized in order to build a basic model. The DUT setup was done together with Vigan Spahiu as well as the operating instructions.

1.5 Outline

Chapter 2 is a chapter where theoretical knowledge is provided, necessary for the understanding of the results and the method used. The topics included are the working principle of a shunt active filter, with the main components and control. Theory of EMC is also touched upon, spectrum analysis and how common mode and differential mode currents appear

A measuring chapter (chapter 3) follows describing the method used when measuring signals from the DUT and specifics around that. How individual components were measured and their values are presented. The lab setup and measuring devices used are listed as well as measured signals from the DUT in operation.

Simulation is a large part of the project and the process and method is explained in chapter 4. Modelling and simulation using the measured component values is explained. Adjustments made to optimize the model are presented and motivated. A comparison of the measurements and the simulations is done and in the discussion, results and the project is evaluated. Finally a conclusion is presented. References are supplied in the final section of the paper.

Chapter 2

Theory

2.1 Shunt active filter

2.1.1 Working principle of a shunt active filter

To eliminate the harmonic content of the load current, the shunt AF injects the inverted harmonics into the connection point of the load in the grid, see figure 2.1. If this is done in phase with the load current harmonics, the line current will appear as only containing the fundamental current components. Reactive power compensation is done similarly, the same amount of reactive current with the opposite sign is injected and thus cancels the unwanted reactive power present in the grid.

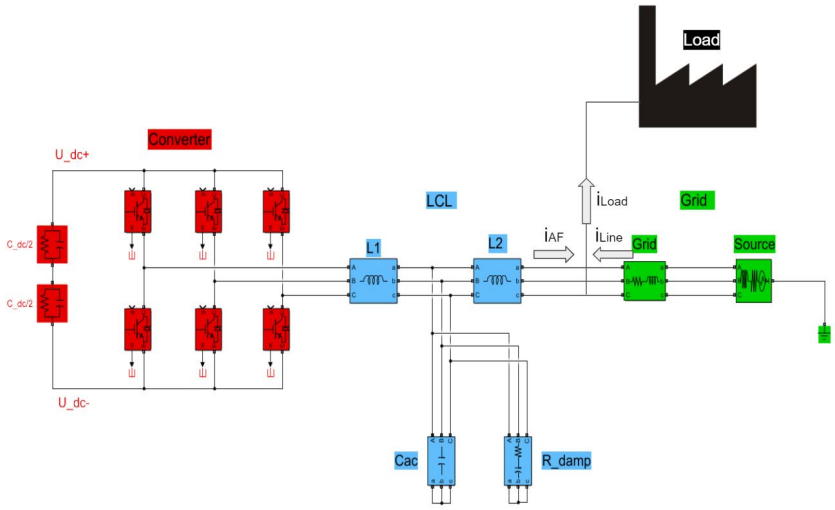


Figure 2.1: Circuit diagram of the shunt active filter placed between the grid and load, made in Simulink. i_{AF} is the injected current.

A mathematical reasoning of the AFs operation follows. If the total load current is considered as the sum of the fundamental current $i_{Load,fund}$ and the harmonic current $i_{Load,harmonic}$, it can be expressed as follows;

$$\vec{i}_{Load} = \vec{i}_{Load,fund} + \vec{i}_{Load,harmonic} \tag{2.1}$$

The harmonic correction current created by the AF is ideally seen as;

$$\vec{i}_{AF} = \vec{i}_{Load,harmonic} \tag{2.2}$$

The operation of the AF becomes clear, as the current created by the AF is inverted and injected it cancels the harmonics in the load current.

$$\vec{i}_{Line} = \vec{i}_{Load} - \vec{i}_{AF} = \vec{i}_{Load,fund} \tag{2.3}$$

The resulting line current only contains the fundamental current and the effects of the e.g switched load, is negligible. In figure 2.2 the AF current can be viewed as an AF filters the load current of a diode rectifier. Injecting the AF current into the load current eliminates the harmonics creating a perfect line current supplied from the grid. The first graph in the figure shows the original load current of the diode rectifier. The second shows the AF current and the final shows a clean line current where the AF has successfully injected the needed current [3, p.16].

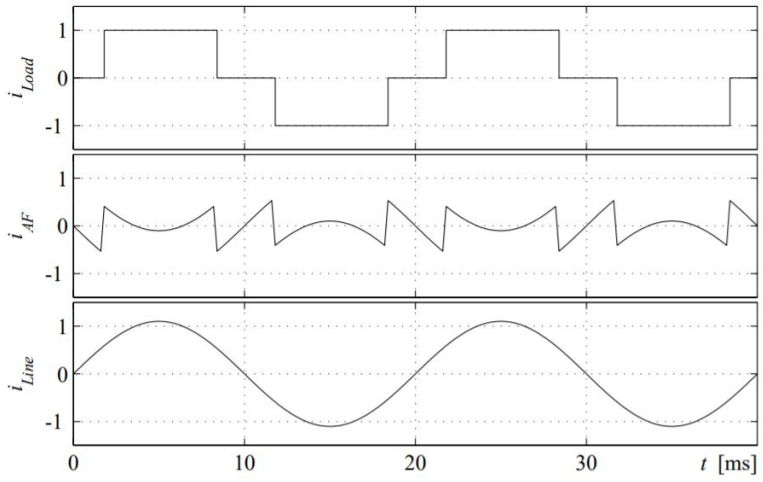


Figure 2.2: Load current at the top, AF current in middle. Line current in the bottom [3, p.16].

2.1.2 Components and construction

Converter

The main component of the active filter is the controllable voltage or current

source. Voltage source converters (VSC) are most commonly used due to ease of installation and their well known topology [10, p.342]. A two level converter has a smaller power loss than an analogue amplifier which makes them more attractive in power electronics [10, p.75]

A three-phase two-level converter, i.e a VSC, uses six IGBTs, two for each phase, see figure 2.1 marked with red. These are used to control the voltage and current flowing in or out of the converter. IGBTs are used as transistors due to their superior forward voltage drop compared to MOSFET. MOSFETs usually have faster switching times however IGBTs can carry much more current in a smaller space, and that's why they are preferred for high power applications. The transistors are each connected to a parallel diode [3] [2].

DC-link capacitor
In combination with the IGBTs the DC link capacitor forms the converter in an AF, see red part of figure 2.1. The DC link capacitor acts as an energy storage. It stores the energy needed to compensate for active power harmonics but still has to have capacity left to absorb unwanted energy in the grid. If the AF is forced to output larger amounts of energy, the stored energy will run out and it has to stop compensating [3].

LCL-filter
Two inductors are combined with a shunt connected capacitor to create a passive line filter, see blue part of figure 2.1. The line filter, or LCL-filter, has several purposes but mainly filters the converters output currents and thus creates a smoother line current. It also attenuates the current ripple from the active filter removing high frequency current components. In addition to the line filter a finer filter is used to attenuate even higher frequency currents. This is commonly called an EMC-filter and might be installed to meet certain legal requirements [3].

2.1.3 Control of machine

Voltage control
To maintain the correct voltage over the DC link capacitor it has to be controlled. This is done by controlling the flow of active phase currents in and out of the converter [3]. By measuring the difference between the actual voltage and the voltage reference over the DC link capacitor, a current reference of the active component of the current vector is calculated that will mitigate the error in the DC-link voltage [8].

Current control
The current controller of an AF operates in the rotating reference frame also known as the dq-system. The current controller uses vector control. To reach the dq-frame, the three phase quantities must firstly be transformed to the alpha-beta frame and from there onward to the dq-frame [8]. The dq-frame is

oriented along the integral of the grid voltage vector, i.e. the "grid flux vector", see figure 2.3. The grid flux vector is located by using a phase locked loop, PLL. In synchronous coordinates, q and d represent the active and reactive power respectively. Hence, two separate controllers can be used to control each quantity as needed. The current controller calculates the voltage reference to be put forward to the transistors using the current reference from the voltage controller. This regulates the current charging or discharging the DC link capacitor [3].

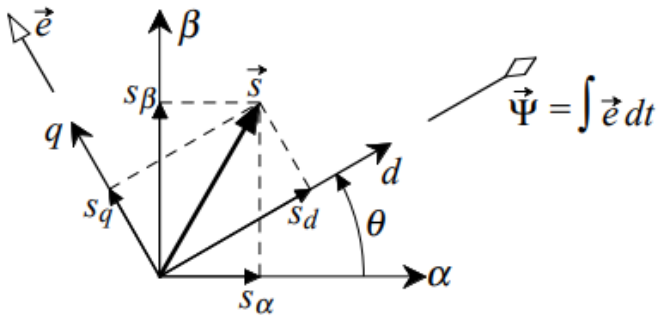


Figure 2.3: The synchronously rotating dq-frame in relationship to the stationary $\alpha\beta$-frame. $\vec{\Psi}$ is the grid flux vector and $\vec{e}$ is the grid voltage vector [3, p.112].

Pulse width modulation

Pulse width modulation or PWM is the control of voltage using switching. The voltage can either be $\frac{U_{dc}}{2}$ or $\frac{-U_{dc}}{2}$ over the transistor, see figure 2.1, depending on if the transistor is on or off. A carrier wave in this case is a repeating triangular wave. A switch is made each time the carrier wave intersects the voltage reference. See figure 2.4. The ratio that the switch is on compared to the total switching period is called a duty cycle, this will give an average voltage that follows the reference voltage. There arises a power loss that originates mainly from the change of switch state. When current flows at the same time as there is still a voltage drop over the IGBT, power is lost through heat. This loss is called switching loss. By separating the switch states with a time period called blanking time, a short circuited DC-link can be avoided.

Modulation with symmetrical reference is used instead of sinusoidal reference to increase the maximum output voltage without over-modulation with 15%. Symmetrical reference gives different harmonic content of the output voltages and currents than sinusoidal reference [8].

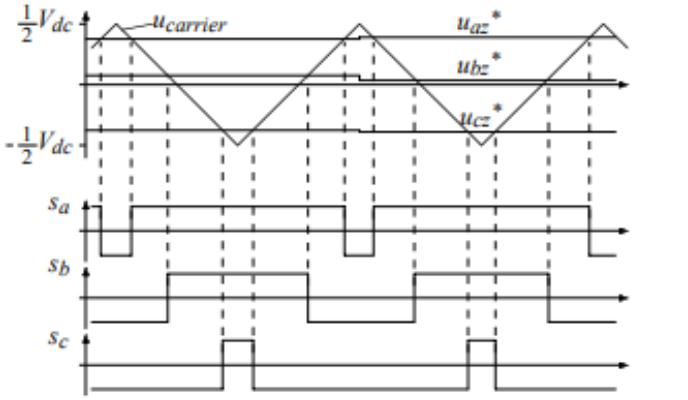


Figure 2.4: Triangular carrier wave Ucarrier, voltage references Uaz*, Ubz* and Ucz* in the top. Switching states in the lower part [3, p.27].

2.2 EMC

2.2.1 What is EMC?

An electromagnetic disturbance that causes a performance degradation in equipment is known as an electromagnetic interference (EMI). It is an electromagnetic pollution that also may disturb transmission channels or systems. To have a clean electromagnetic surrounding all devises have to follow regulations. This is where EMC can be introduced. Electromagnetic compatibility, EMC is the result of treating EMI as a serious threat, that needs to be suppressed. Fulfillment of EMC regulations means a limitation of disturbances caused by electromagnetic emission. Electromagnetic emissions are still present but levels and frequencies are regulated to ensure that the devices will not interfere with each other. These regulations refer to a maximum of conducted voltage, conducted current, radiated magnetic field or radiated electric field. Leakage of conducted currents into the grid often originates from lack of insulation between the circuit and earth, this is a parasitic component. It gives the currents a path that is not intended which might have consequences on electronics nearby [16, p.3].

2.2.2 Rules and regulations

There are different regulations for various countries, but many areas use similar standards to make it easier to set up tests. The CE-mark indicates that the product passes many requirements, which one of them indicates conformity with the EMC Directive 2014/30/EU. Conducted emissions are measured between the frequencies 150kHz-30MHz, while the radiated emissions are measured for 30MHz-1GHz [16, p.38-41].

2.2.3 Parasites

Parasitic elements
Usually passive electrical components such as resistors and capacitors are used as ideal circuit elements. However, all real components will inevitably house resistance, inductance and capacitance. These unwanted elements are called parasitic elements. In all conducting materials, resistive and inductive characteristics will be present. Conducting materials in close proximity to each other will experience a capacitive coupling. These elements can usually be disregarded except when reaching higher frequencies. Frequency behavior of inductors and capacitances can be described with the following equations. These show how, for example, a parasitic capacitance will result in a small impedance (X_C) allowing currents to flow through the capacitance at higher frequencies. Parasitic inductances behave in the complete opposite way.

$$X_C = \frac{1}{j2\pi fC} \quad \text{and} \quad X_L = j2\pi fL \tag{2.4}$$

How severely components are affected by parasitic elements largely depends on their internal structure. For example, a wire wound resistor in figure 2.5 consists of a resistive wire wound around a core and will naturally act as an inductance at higher frequencies with its coil like structure [14].

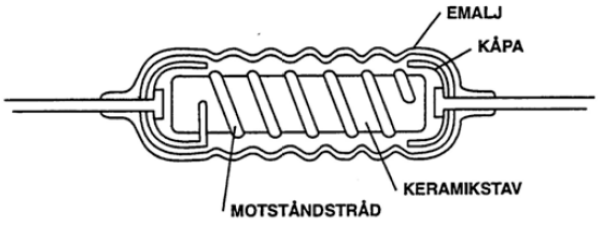


Figure 2.5: Intersection of a wire wound resistor, the resistive wire (motståndstråd) is wound around the core (keremikstav) [12].

Equivalent circuit
When modelling a component where the high frequency behavior is of interest, the parasitic elements must be taken into account. By adding the parasitic elements to the model an equivalent circuit is created, representing the non-idealities of the component. Simpler equivalent circuits are of the first order and use one inductance and one capacitance. To include very high frequency behavior higher order models must be used, i.e. using multiple inductances and capacitances.

Capacitor
For example, when modeling a capacitor the parasitic elements are included and thereby affect the high frequency behavior. A first order model might be modeled as in figure 2.6 [9].

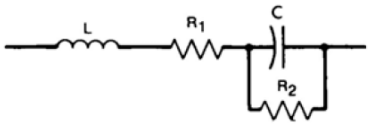


Figure 2.6: Equivalent diagram of a paper capacitor [12].

The equivalent series inductance, (ESL), and the equivalent series resistance, (ESR), are the results of the conducting material being non ideal. The parallel resistance is equal to the resistance through the dielectric material being used [9].

Inductor
Inductors are usually constructed by winding wires around a core into a coil configuration in some form. As the number of turns around the core are many and thus causing the length of the wire to be long, some ESR is added to the equivalent circuit [14]. A parallel capacitance arises as the windings of the coil are in close proximity to each other and together create a parallel capacitance over the inductor. An equivalent circuit of a coil can be seen in figure 2.7 [11].

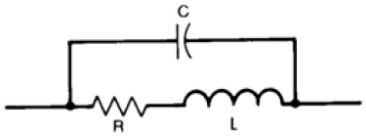


Figure 2.7: Equivalent diagram of a coil [12].

Impedance curve
The equivalent circuit of a component determines the impedance curve. A simple capacitor has a characteristic impedance Z that decreases as the frequency increases until the resonance frequency F_{res} is reached. Frequencies higher than F_{res} gives an increased impedance Z. The opposite effect is found for the inductance as seen in figure 2.8.

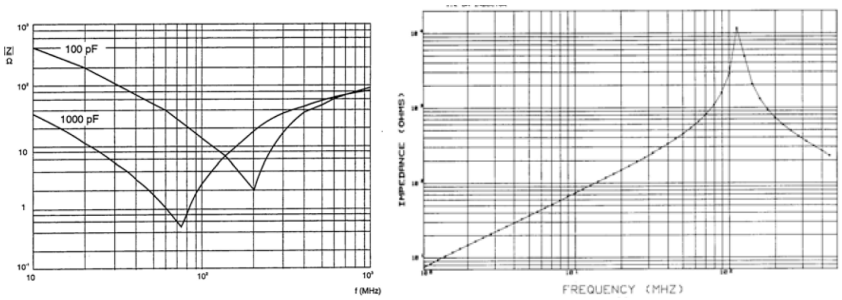


Figure 2.8: Characteristic impedance of a capacitor to the left, and inductor to the right [12].

A cable also contains parasitic elements, thus it can be modelled as a LCR network or an equivalent circuit. Depending on the length of the cable, repetitions of L', C' and R' may need to be added in figure 2.9.

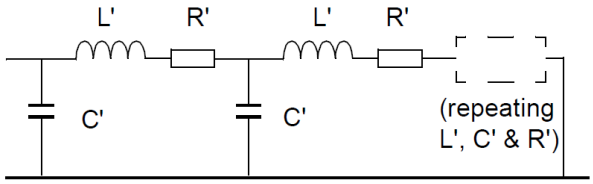


Figure 2.9: Equivalent circuit model of a cable, where the total inductance is the sum of L', and the total capacitance is the sum of C' [16, p.266].

This type of equivalent circuit model determines the characteristic impedance Z as seen in figure 2.10

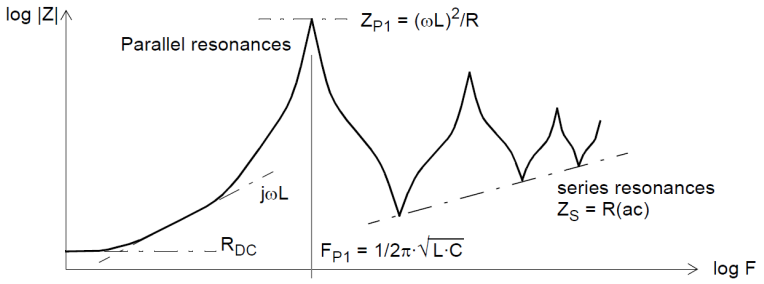


Figure 2.10: Characteristic impedance Z of a cable for frequency F [16].

As seen, the characteristic impedance can be very complex for higher frequencies depending on the added elements in the circuit. The resonance frequency is found using the following equation:

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{LC}} \tag{2.5}$$

An impedance analyser can be used to measure the impedance Z of a component over a frequency spectrum. This measurement can be used to fit an equivalent circuit that matches the impedance. Thereafter the equivalent circuit's impedance curve can be simulated and verified. As seen in figure 2.9 and 2.10, the equivalent circuit has to be more complex i.e of a higher order, to fit a curve with many resonance frequencies. Therefore it is easier to match a low frequency impedance curve than a high frequency curve to an equivalent circuit [16].

2.2.4 Common- and differential mode

When discussing EMI, the concepts of common- and differential mode are fundamental to understanding the coupling of EMI to the device.

Differential mode
In an ideal three phase system the sum of the phase currents is always zero. When a differential mode current appears, it affects the currents of a phase but the disturbing current components is lead back through the other phases. This results in a phase current sum still being zero. In figure 2.11 the cable connecting the two electric circuits carries differential mode currents (Go and return) through the wires in the cable. From the figure it is clear that the current sum flowing in the cable is zero. Differential mode currents can be induced by radiated electromagnetic emissions but can be suppressed through proper design by minimising the wire loops as much as possible [16].

Common mode
When a common mode interference occurs in a three phase system, it affects all phases. The sum of the currents flowing in the phases is no longer zero. The remaining current, i.e the common mode current, then uses parasitic couplings to ground to make its way back into the grid. Notice in figure 2.11 that parasitic capacitances and inductances from the device to the signal-ground play an important role in the common mode coupling circuit. These parasitic elements largely determine the amplitude and frequency of the interference affecting the device [16].

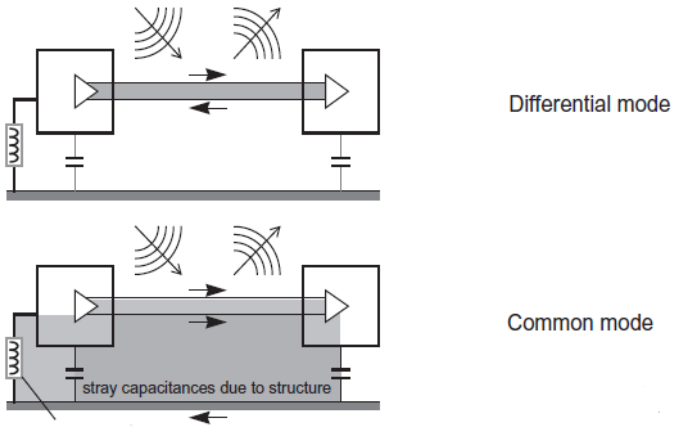


Figure 2.11: Go and return current paths of two connected components over ground, differential mode and common mode. Loop area marked gray [16].

2.2.5 Voltage and current spectrum

A common cause for EMI is switched electronics. Switching creates square waves that are very rich in harmonic frequencies. The ideal square wave has an infinitely fast rise and fall time. This produces an infinitely high frequency harmonic content made out of odd harmonics such as 3x, 5x, 7x, ... the square wave frequency reaching infinitely high frequencies.

In order to visualize the frequency content of any signal the Fourier transform is used. This transforms the signal into the frequency domain. Different waveforms have different frequency content. The frequency content of some recognisable waveforms are shown in figure 2.12 [16].

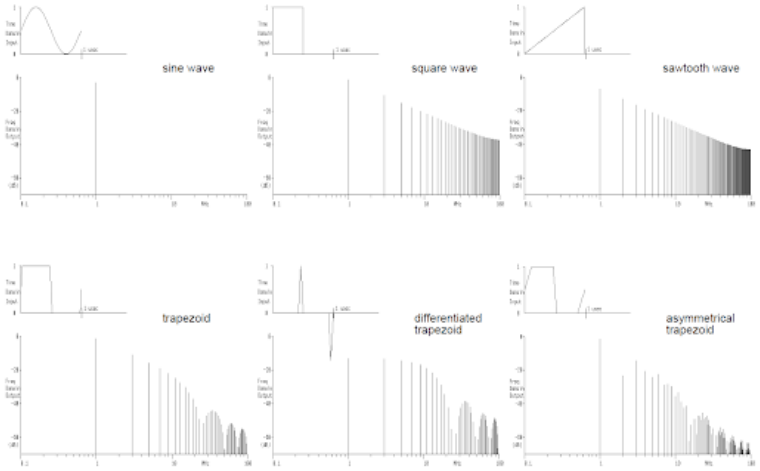


Figure 2.12: Different types of waves and their harmonic content in frequency domain [16, p.290].

As seen in figure 2.12 a transient produces more harmonic content than a single sinusoidal signal, which produces no harmonic content except for its own frequency. Slower rise times or rounder wave appearance gives more suppressed harmonics at higher frequencies. It is therefore better to use as slow logic family as possible to avoid fast switches that will contribute to electromagnetic emission [16]. The logarithmic ratio between two quantities can be represented with deciBel (dB). The ratio can be calculated using a voltage or current across a constant impedance, it is given by:

$$dBV = 20 * log_{10}\frac{V_1}{V_2} \quad \text{or} \quad dB = 20 * log_{10}\frac{I_1}{I_2} \tag{2.6}$$

[16, p.516] , where V_1 is the measured voltage and V_2 is the reference voltage, I_1 is measured current and I_2 is the reference current.

Chapter 3

Measurements

This chapter contains measurements on component and system level required to build a high frequency model. The device under test,(DUT), was an active filter supplied by Comsys AB. The DUT was set up and run in IEAs lab 6 at LTH. Operation of the DUT was done through Comsys control portal. The circuit seen in figure 3.1 contains the main components of the shunt active filter. The red part is the converter which contains the IGBTs and the DC capacitance C_{dc}. The blue part is the LCL-filter which contains the inductances L1, L2 and the filter capacitor Cac. A dampening resistance R_{damp} is connected in parallel with Cac. The green part is the grid and source.

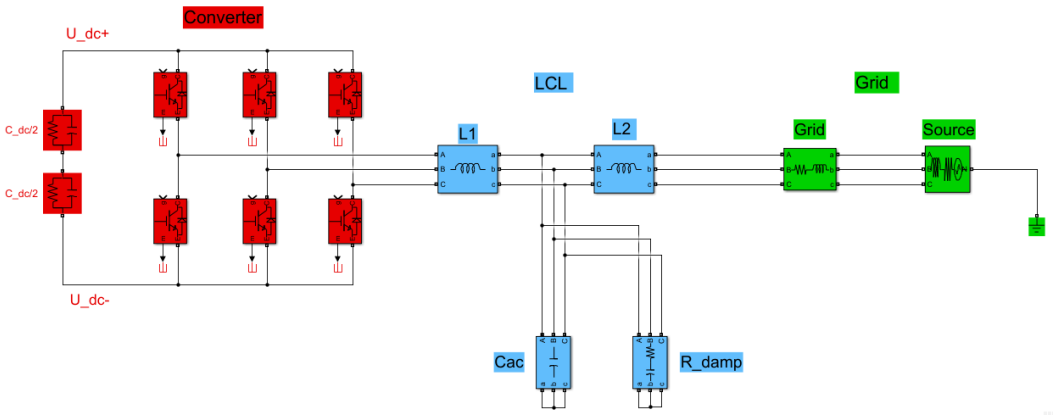


Figure 3.1: Circuit diagram of the shunt active filter, made in Simulink.

3.1 Measurement on component level

The impedance of the components were measured with a HP 4194A impedance analyser that can sweep over a frequency spectrum of 100Hz-40MHz. The analyzer can fit a first order equivalent circuit to the impedance measurement. Five different equivalent circuits can be chosen. Although the number of circuits is quite low, the available circuits are versatile and a good match could usually be found for frequencies up to 10MHz. The equivalent circuits impedance could be simulated and plotted next to the measurement to ensure the match.

The DUT was disassembled to measure the impedances for the separate components. The cables used to measure the components were made as short as possible to avoid parasitic elements from the measuring equipment. They were also twined to minimise differential mode interference. Parasitic elements of 1.97pF and 145.9nH could be traced to the measuring cable setup. The frequency spectrum was chosen to 100Hz-10MHz. This gave an adequate measurement that didn't contain equipment parasitics which originated from the measurement cables at higher frequencies.

To measure the parasitic elements of the IGBT to ground, the component had to be dissected. One IGBT module contains two IGBTs in series, and when measuring from either the DC+, DC- or AC terminal to baseplate/ground, all capacitances are in parallel. To measure the impedance separately from the DC+, DC- or AC terminal to baseplate, the bond wires had to be cut. The separation of wires can be seen in figure 3.2 as four red lines.

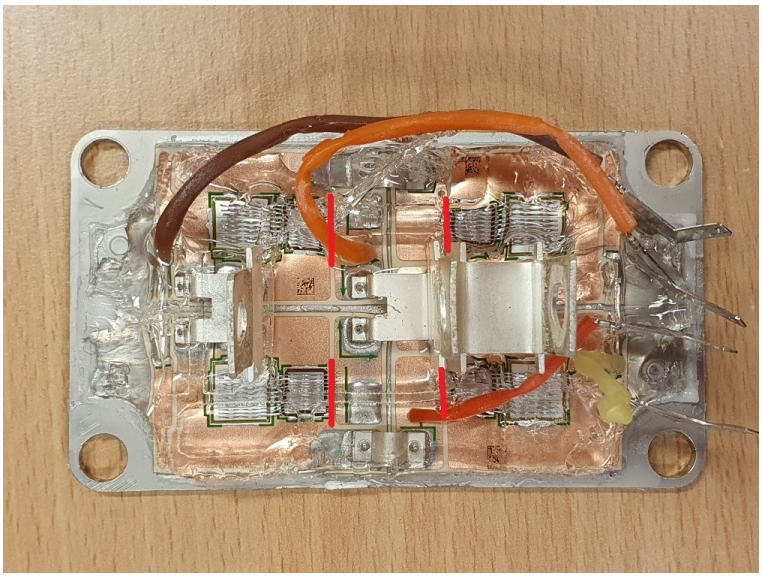
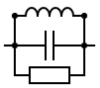
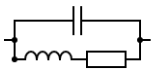
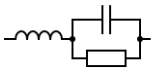
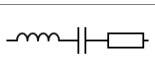
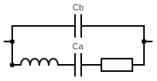


Figure 3.2: Opened IGBT, red marked lines were the bond wires to be cut.

The parasitic elements of the components were measured, both over the

component and at the terminal of the component to ground. The impedance curve was plotted and a first order equivalent circuit was chosen to get a good simulated fit. An example of an impedance measurement can be seen in figure 3.3. This is a measurement of a IGBT DC+ terminal to ground, used in the DUT. There is a choice of five different equivalent circuits using L, R and C named A-E. The circuits of interest can be seen in table 3.1:

Table 3.1: Equivalent circuit available in the HP4194a impedance analyzer.

	A	$L\|\|C\|\|R$
	B	$C\|\|(L+R)$
	C	$L+(C\|\|R)$
	D	$(L+C+R)$
	E	$Cb\|\|(L+Ca+R)$

The best equivalent circuit was chosen to plot a good simulation, in this case, a series LCR circuit. The impedance measurement seen in the middle of figure 3.3 is the thick yellow curve, and very close is the fitting from the equivalent circuit as the pale yellow curve. The blue curve is the phase angle, with its fitting, the pale blue curve.

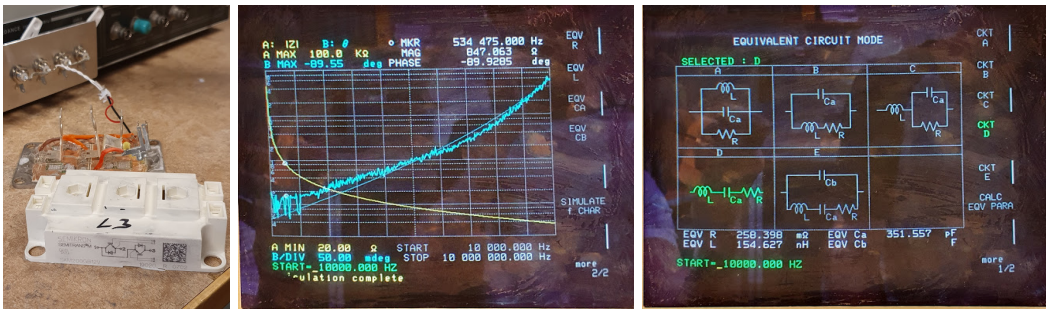


Figure 3.3: Left: the IGBT measuring setup. Middle: the measured and simulated impedance and phase curves. Right: Equivalent circuit of a IGBT DC+ terminal to ground in the DUT. There are 5 different equivalent circuits to choose from, named A, B, C, D and E.

These measurements were made for most components, and the equivalent circuit that fits the best was chosen. The start frequency of the sweep was either 100Hz or 10kHz depending on how well the simulation could fit the measurement, stop frequency was always 10MHz. Tables 3.2, 3.3 and 3.4 display the measured values and the chosen equivalent circuits.

Table 3.2: Type of equivalent circuit, with values of LCR over the measured component.

Component	L1	L2	Cac	C_{DC}
Equivalent circuit	$L\|\|C\|\|R$	$L\|\|C\|\|R$	$(L+C+R)$	$(L+C+R)$
Start frequency	10kHz	10kHz	100Hz	10kHz
Inductance (L)	[redacted]	[redacted]	214nH	151nH
Capacitance (Ca)	84.0pF	13.7pF	[redacted]	[redacted]
Resistance (R)	7.52kΩ	2.98kΩ	165mΩ	98.8mΩ

Table 3.3: Type of equivalent circuit, with values of LCR for the LCL-filter parasites to ground.

To ground	L1	L2	Cac
Equivalent circuit	$Cb\|\|(L+Ca+R)$	$Cb\|\|(L+Ca+R)$	$Cb\|\|(L+Ca+R)$
Start frequency	10kHz	10kHz	100Hz
Inductance (L)	45.9mH	60.7µH	637µH
Capacitance (Ca)	119fF	12.2pF	284fF
Capacitance (Cb)	2.84pF	29.1pF	21.1pF
Resistance (R)	83.3kΩ	489Ω	18.4kΩ

Table 3.4: Type of equivalent circuit, with values of LCR for converter parasites to ground.

To ground	IGBT (AC)	IGBT (DC+)	IGBT (DC-)	C_{DC}
Equivalent circuit	$(L+C+R)$	$(L+C+R)$	$(L+C+R)$	$(L+C+R)$
Start frequency	10kHz	10kHz	10kHz	100Hz
Inductance (L)	155nH	155nH	150nH	149nH
Capacitance (Ca)	418pF	352pF	76.4pF	77.9pF
Resistance (R)	266mΩ	258mΩ	364mΩ	13.8Ω

3.2 Measurement on system level

The DUT installed in lab 6 was modified slightly to increase the observability of the non-idealities. The EMC-filter was bypassed to ensure that the disturbances would not be attenuated. To be certain that the measured signals contained as little disturbances from the surrounding as possible an isolating transformer was used. The transformer supplied power to the computer and the interface on the DUT. No asymmetric or non-linear loads were intentionally connected to the grid for the AF to compensate and thus it was idling. The DC voltage was set to 850V.

A picoscope 4444 was used to collect the measured data with a bandwidth of 20MHz [17]. Sampling was done at 16MS/s. (Mega Sample per second). To be able to measure signals at higher frequencies adequate measurement tool bandwidths were used. A differential voltage probe, Tektronix p5200a, with a bandwidth of 50MHz was used [18].

As the believed common mode "drivers" were the IGBTs and converter module, measurements of signal levels were focused around this part of the DUT. Voltage across the DC link capacitor, and voltages from the positive and negative side to the grounded chassi were measured. The voltage output on the AC side of the converter was measured in relation to the chassi as well. Current through the line filter inductor L1 was measured using a current probe with a bandwidth of 100kHz. The measurement points are shown in figure 3.4.

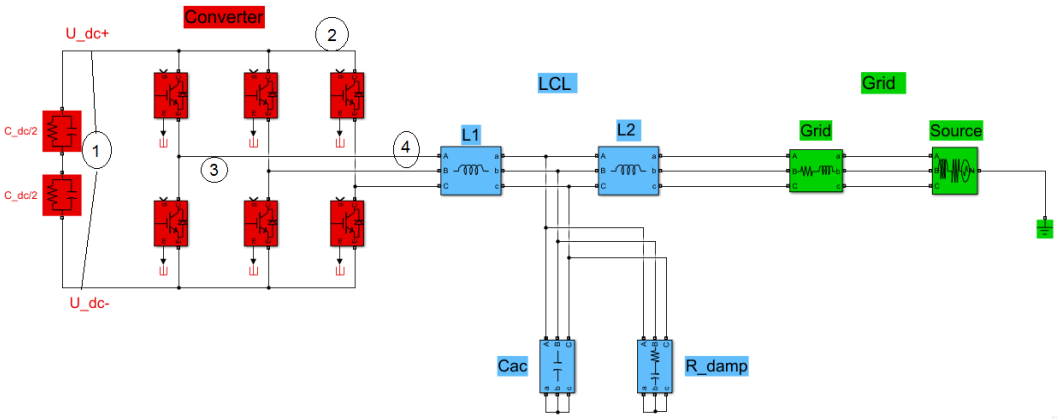


Figure 3.4: Circuit diagram of the shunt active filter showing the four measurement points. 1: UDC+ to UDC-, 2: UDC+ to ground, 3: AC output voltage, 4: L1 current. Made in Simulink.

3.2.1 DUT measurements

The following measurements are from the setup in lab 6 using the equipment described earlier. The y-axis of the FFT figures is expressed as magnitude, (Mag). This is the the logarithm of the the measured value divided by the reference "1". Represented as dB using equation 2.6, it can be viewed as:

$$dBV = 20 * log_{10}\frac{V_1}{1} = 20 * Mag \quad \text{or} \quad dB = 20 * log_{10}\frac{I_1}{1} = 20 * Mag \quad (3.1)$$

UDC+-

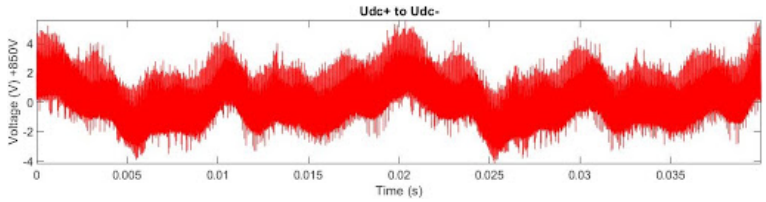


Figure 3.5: Udc+ to Udc-, over a time period of 40ms. The signal is measured as AC, meaning 0V = 850V Measured on point 1 of the DUT, see figure 3.4.

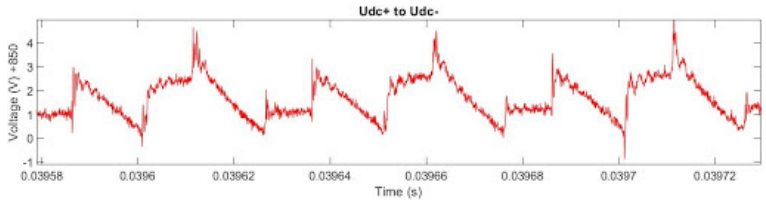


Figure 3.6: Udc+ to Udc-, plotted for a time window corresponding to 3 modulation periods (150µs). The signal is measured as AC, meaning 0V = 850V. Measured on point 1 of the DUT, see figure 3.4.

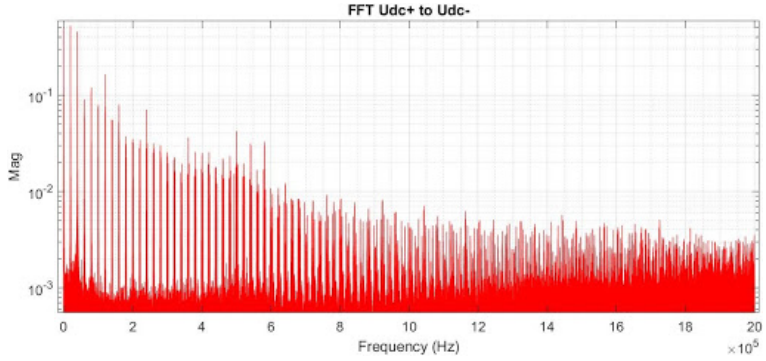


Figure 3.7: FFT calculation of Udc+ to Udc- up to 2MHz. The sampling time was 60ns and a total of 667k samples were used. Measured on point 1 of the DUT, see figure 3.4.

UDC+ to ground

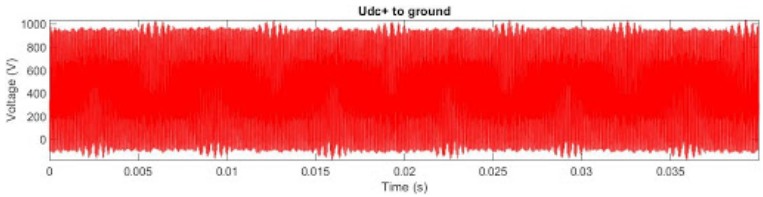


Figure 3.8: Udc+ to ground, over a time period of 40ms. Measured on point 2 of the DUT, see figure 3.4.

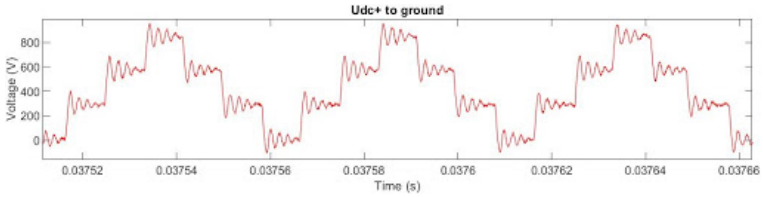


Figure 3.9: Udc+ to ground, plotted for a time window corresponding to 3 modulation periods (150µs). Measured on point 2 of the DUT, see figure 3.4.

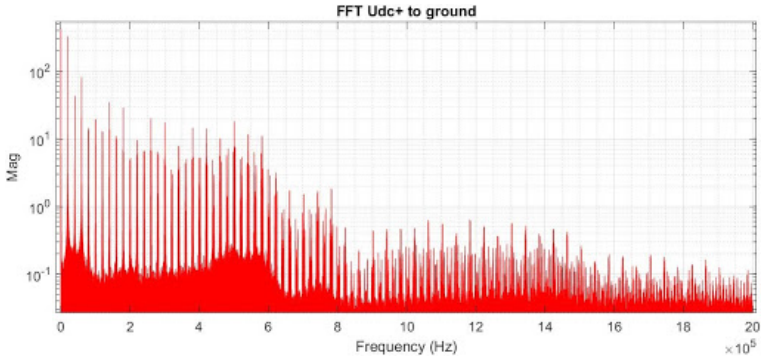


Figure 3.10: FFT calculation of Udc+ to ground up to 2MHz. The sampling time was 60ns and a total of 667k samples were used. Measured on point 2 of the DUT, see figure 3.4.

AC output voltage

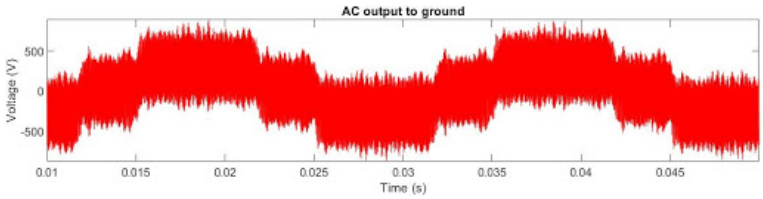


Figure 3.11: AC output to ground, over a time period of 40ms. Measured on point 3 of the DUT, see figure 3.4.

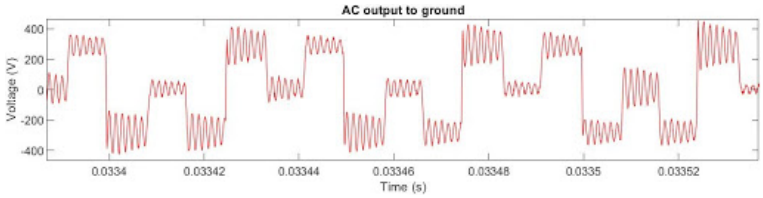


Figure 3.12: AC output to ground, plotted for a time window corresponding to 3 modulation periods (150µs). Measured on point 3 of the DUT, see figure 3.4.

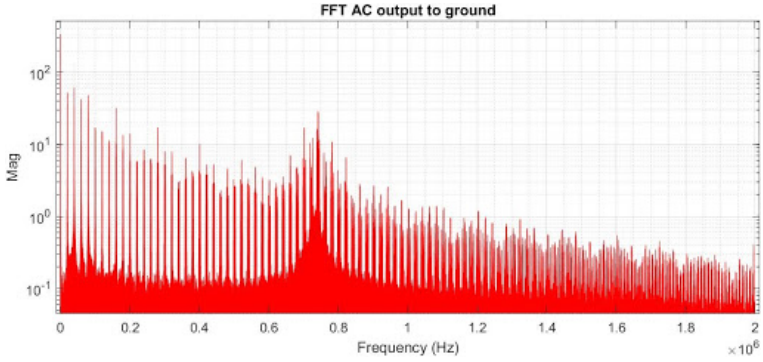


Figure 3.13: FFT calculation of AC output up to 2MHz. The sampling time was 60ns and a total of 667k samples were used. Measured on point 3 of the DUT, see figure 3.4.

L1 current

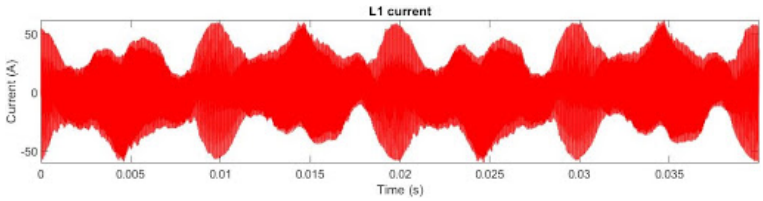


Figure 3.14: L1 current, over a time period of 40ms. Measured on point 4 of the DUT, see figure 3.4.

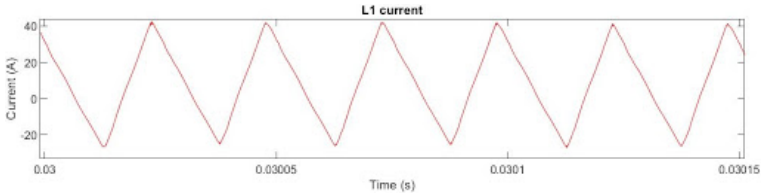


Figure 3.15: L1 current, plotted for a time window corresponding to 3 modulation periods (150µs). Measured on point 4 of the DUT, see figure 3.4.

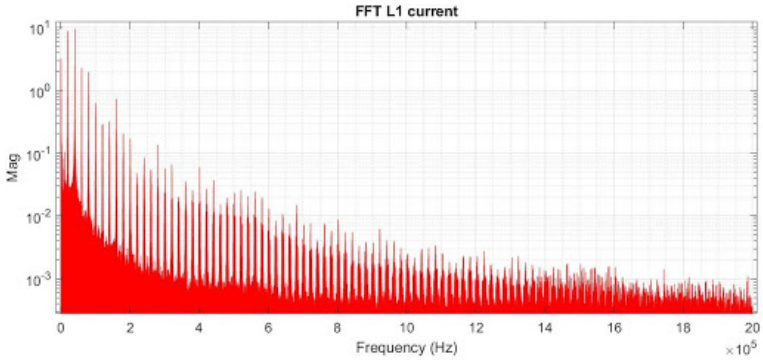


Figure 3.16: FFT calculation of L1 current up to 2MHz. The sampling time was 60ns and a total of 667k samples were used. Measured on point 4 of the DUT, see figure 3.4.

When viewing the signal of all measurements with a time period of 40ms (figures: 3.5, 3.8, 3.11 and 3.14), recurring patterns can be recognized. This means that the patterns of all four measured signals that are zoomed in depend on where they are zoomed in. This has to be taken into consideration when later making comparisons between measured and simulated signals.

Important data can be extracted from the zoomed in Udc+ to ground voltage measurement (figure 3.9) and the FFT (figure 3.10). The dampening of the oscillations at the four voltage levels is 0.69, and the frequency of these oscillations is 540kHz. This frequency is also found as a peak in the FFT figure 3.7 of Udc+ to Udc-. Furthermore oscillations can be found at the AC output voltage with a frequency of 740kHz (figure 3.12 and 3.13).

3.3 Common mode current

Measuring the Common mode, CM, currents meant measuring the current flowing through the electric ground cable connecting the chassi of the DUT to the grid ground. The CM signals were expected to be small and might be overshadowed by surrounding disturbances picked up in the current probe. Some measures were therefore taken to limit the overhearing. As the current clamp measures the magnetic field created by a nearby current to calculate the current itself, the ground cable had to be isolated from other cables as much as possible. This was done by leading the current through a longer cable and measuring it some distance from the AF where most of the radiated disturbances would not reach. But total isolation was not possible and minor overhearing might be found in the measurements.

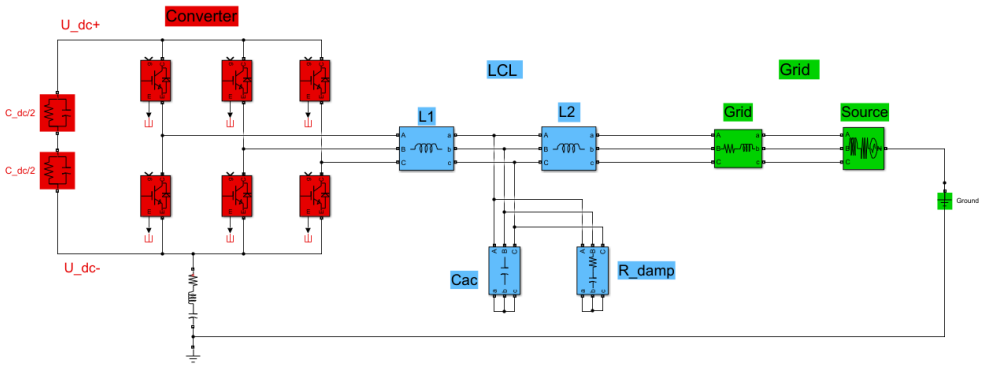


Figure 3.17: Circuit diagram of the shunt active filter showing the an example of common mode current path through ground. Made in Simulink.

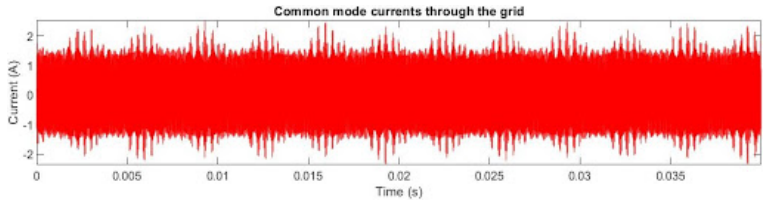


Figure 3.18: Common mode current, over a time period of 40ms. Measured in the ground cable connecting the DUTs chassi to grid ground, see figure 3.17.

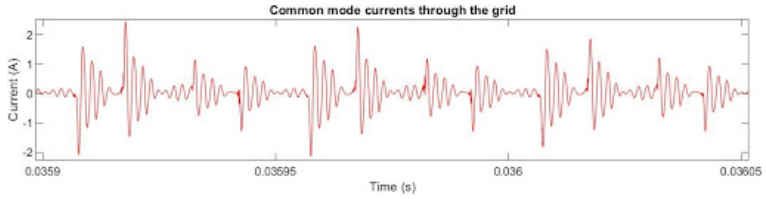


Figure 3.19: Common mode current, plotted for a time window corresponding to 3 modulation periods (150µs). Measured in the ground cable connecting the DUTs chassi to grid ground, see figure 3.17.

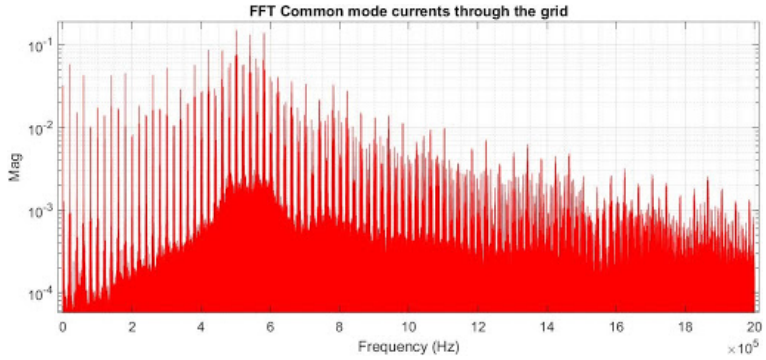


Figure 3.20: FFT calculation of the common mode current up to 2MHz. The sampling time was $60ns$ and a total of 667k samples were used. Measured in the ground cable connecting the DUTs chassi to grid ground, see figure 3.17.

Chapter 4

Model building and simulation

4.1 Modelling in Simulink

To simulate the AF a model from Comsys AB was used as a foundation. The simulation time resolution was increased to 40MS/s from the former 4MS/s. Using the higher resolution, high frequency signals could be analysed.

The AF was simulated as it was run, idling without load. The reference voltage over the DC-link capacitor was held at 850V and the PWM used symmetric modulation. The low frequency operation of the model was verified before parasitic elements were added.

Unfortunately an error in the model causes the voltage in Udc to unexpectedly jump or drop at the "peak" of the Udc to ground simulation, see 4.1. The error seemed to be a switching error at first glance but the switching control signal to the IGBTs did not show any signs of producing a faulty signal. Efforts were made to trace down the disturbance causing the error but with no luck. The error is unfortunate and will impact the simulation and results in some way. Comparisons can nevertheless still be done by focusing on the satisfactory parts where no error is present.

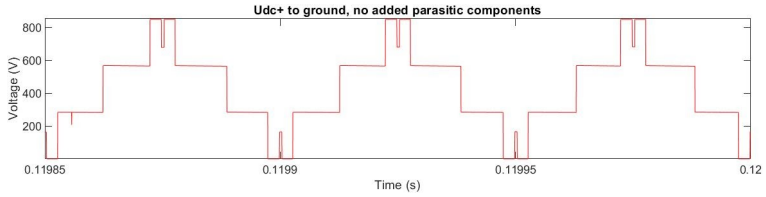


Figure 4.1: Udc+ to ground, plotted for a time window corresponding to 3 modulation periods (150µs). Simulated without any added equivalent circuits and parasitics. Showing the unexpected jump or drop at the peak.

The parasitic elements and the equivalent circuit measured and fitted from the impedance analyser were added to the Simulink model. Measuring points to view the currents flowing through the parasitic elements were also added. The complete model can be seen in figure 4.2.

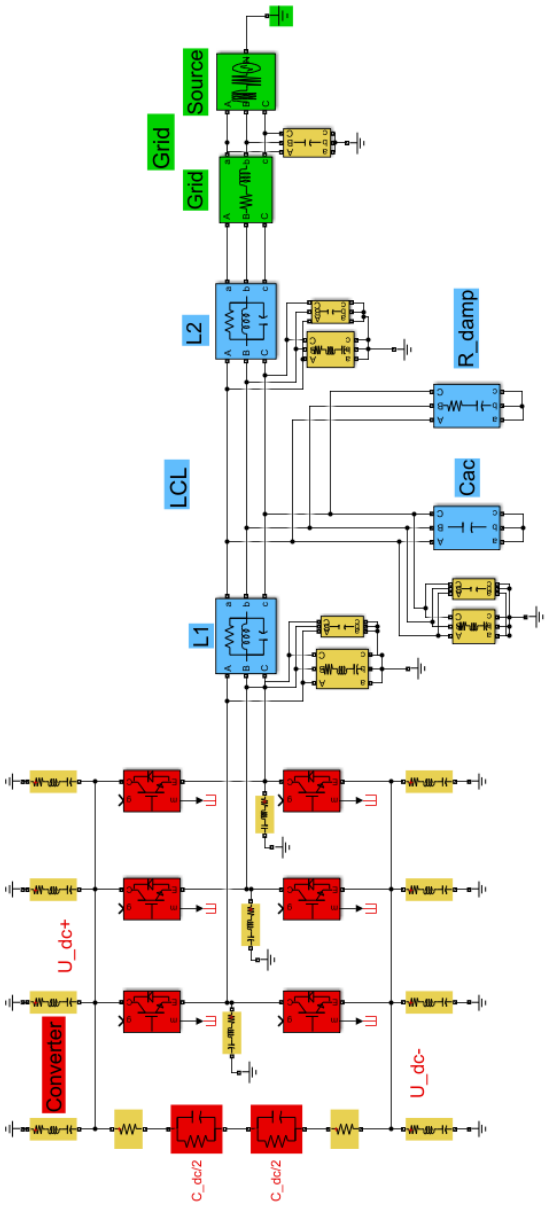


Figure 4.2: Model with parasitic elements (yellow) added. Made in Simulink.

4.1.1 Simulated results using measured values

The following simulations use the measured component values from the impedance analyser.

UDC+-

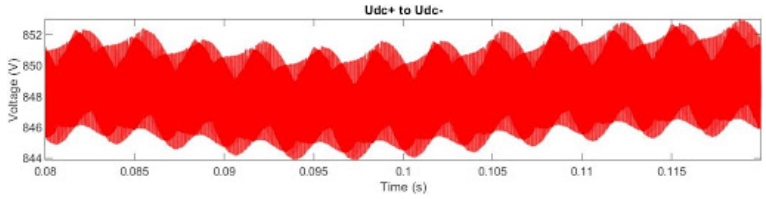


Figure 4.3: Udc+ to Udc-, over a time period of 40ms. The circuit is not tuned. Measuring point 1, see figure 3.4.

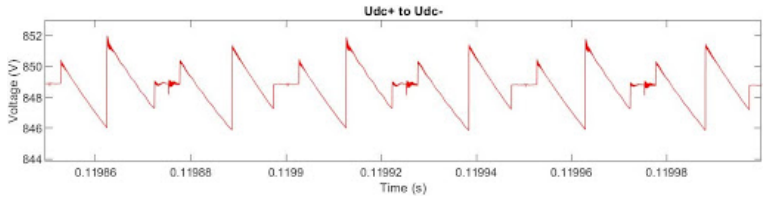


Figure 4.4: Udc+ to Udc-, plotted for a time window corresponding to 3 modulation periods (150µs), the circuit is not tuned. Measuring point 1, see figure 3.4.

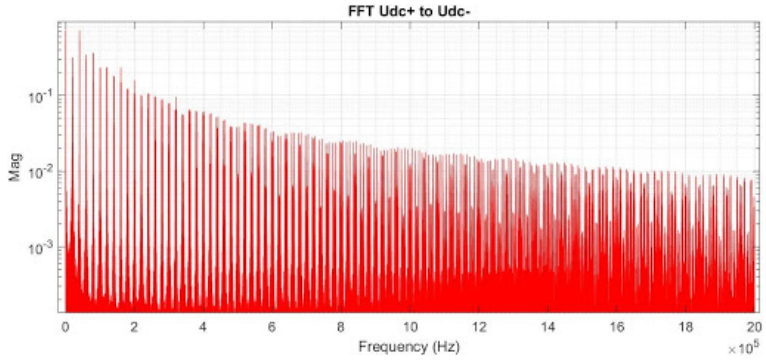


Figure 4.5: FFT calculation of Udc+ to Udc- up to 2MHz. The sampling time was $25ns$ and a total of 1.6M samples were used. The circuit is not tuned. Measuring point 1, see figure 3.4.

UDC+ to ground

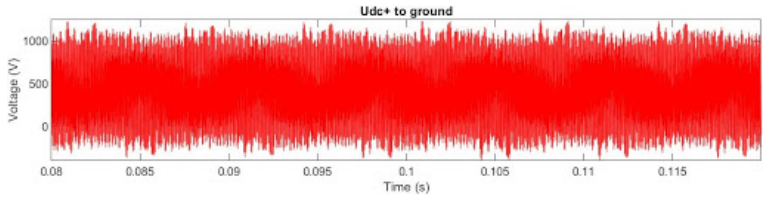


Figure 4.6: Udc+ to ground, over a time period of 40ms. The circuit is not tuned. Measuring point 2, see figure 3.4.

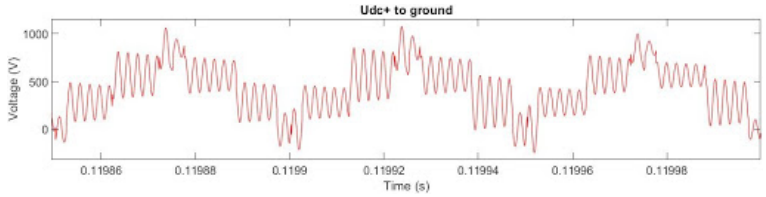


Figure 4.7: Udc+ to ground, plotted for a time window corresponding to 3 modulation periods (150µs). The circuit is not tuned. Measuring point 2, see figure 3.4.

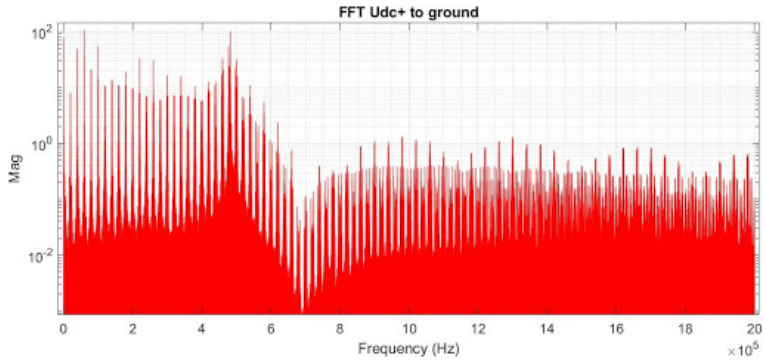


Figure 4.8: FFT calculation of Udc+ to ground up to 2MHz. The sampling time was $25ns$ and a total of 1.6M samples were used. The circuit is not tuned. Measuring point 2, see figure 3.4.

AC output voltage

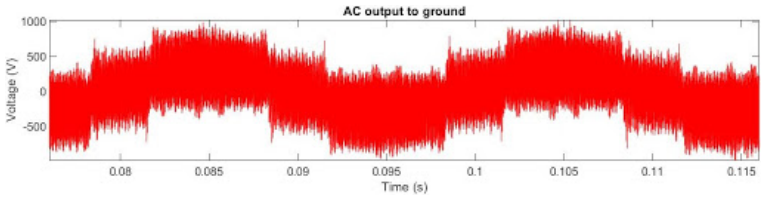


Figure 4.9: AC output voltage to ground, over a time period of 40ms. The circuit is not tuned. Measuring point 3, see figure 3.4.

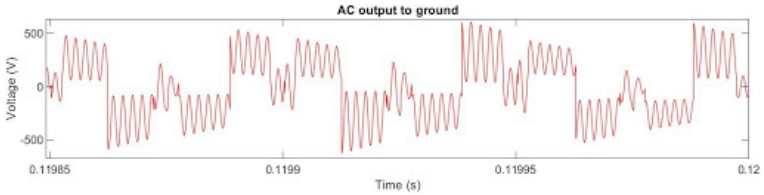


Figure 4.10: AC output voltage to ground, plotted for a time window corresponding to 3 modulation periods (150µs). The circuit is not tuned. Measuring point 3, see figure 3.4.

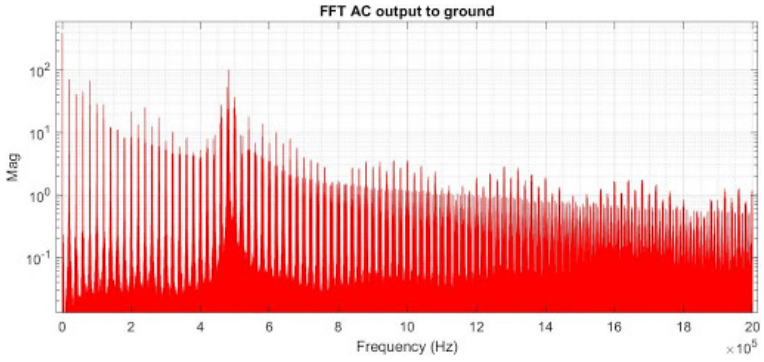


Figure 4.11: FFT calculation of AC output voltage up to 2MHz. The sampling time was $25ns$ and a total of 1.6M samples were used. The circuit is not tuned. Measuring point 3, see figure 3.4.

L1 current

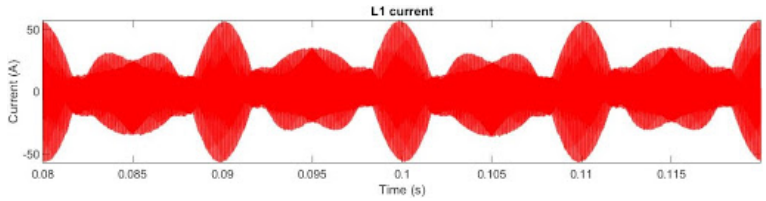


Figure 4.12: L1 current in the time domain, simulated for 40ms. The circuit is not tuned. Measuring point 4, see figure 3.4.

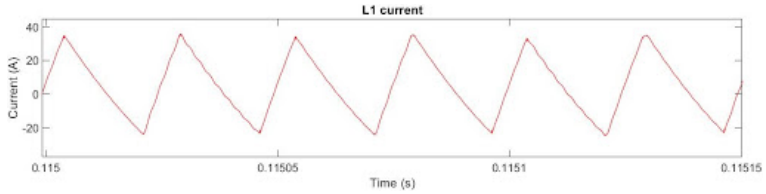


Figure 4.13: L1 current in the time domain, plotted for a time window corresponding to 3 modulation periods (150µs). The circuit is not tuned. Measuring point 4, see figure 3.4.

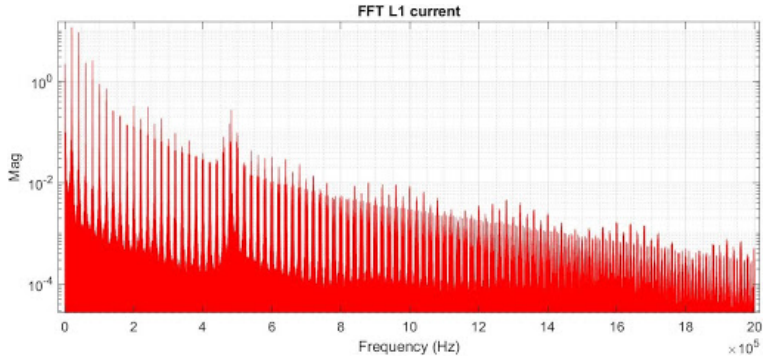


Figure 4.14: FFT calculation of L1 current up to 2MHz. The sampling time was $25ns$ and a total of 1.6M samples were used. The circuit is not tuned. Measuring point 4, see figure 3.4.

4.1.2 Results from simulation using measured values

When comparing the simulation to the measured signals some similarities and dissimilarities are worth analysing. Oscillations in "UDC+ to ground" are present in both the measured and the simulated signals, see figures 3.9 and 4.7. The measured and simulated signals have frequencies of 540kHz and 480kHz respectively. This implies that the inductive and the capacitive values introduced by the parasitic elements are almost correct. This is also seen in the fast Fourier transform where a peak is located at ca 500kHz for both measured and simulated signals, see figures 3.10 and 4.8. However the damping, is weaker in the simulation compared to the measured signal in the lab. When measuring, the damping coefficient is 0.69 while being 0.96 when simulating. In figures 3.12 and 4.10 difference in frequency is clear between measurements and simulation. These differences will be analyzed and discussed in chapter 5.

4.2 Modelling with calibrations

4.2.1 Tuning

To further improve upon the model the parasitic values were tuned. Using equation 2.5 that describes resonance frequencies, it is seen that to decrease the frequency difference between the simulated and measured signals, the total L and C product should be decreased. This would raise the resonance frequency in the simulation. Knowing which components that should be tuned was difficult but using the resonant frequency equation 2.5 and component values, the active components causing the oscillation could be distinguished. Simplifying the circuit to a series resonant circuit, the active components where energy can oscillate back and forth seemed to be the line filter inductor L1 and the parasites to ground in the converter, see figure 4.15. This implies that to improve upon the model, the parasitic elements connecting the converter to ground should be modeled slightly smaller.

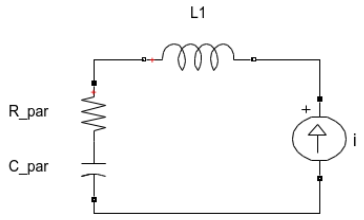


Figure 4.15: Series resonant circuit containing the converter parasites and the inductor L1.

To get a better match between the simulated and measured oscillations in "UDC+ to ground" the parasitic inductances and capacitances from the con-

verter had to be lowered by 20%. This increases the resonant frequency of the LCR resonant circuit resulting in higher frequency oscillations in the simulation.

To match the damping of the measured signal (figure 3.9) in the simulation (figure 4.7), a resistive element was added. To achieve the needed damping a resistance of 70Ω was inserted in series with the parasites measured at Udc+ to ground and at Udc- to ground.

4.2.2 Simulated results using tuned values

The following simulation use the tuned component values.
Udc+-

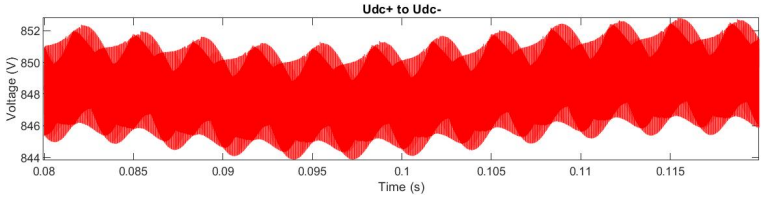


Figure 4.16: Udc+ to Udc- over a time period of 40ms. The circuit is tuned. Measuring point 1, see figure 3.4.

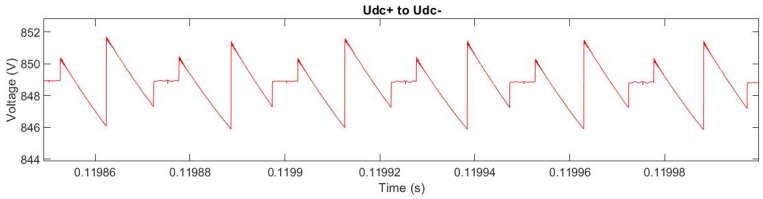


Figure 4.17: Udc+ to Udc-, plotted for a time window corresponding to 3 modulation periods (150µs). The circuit is tuned. Measuring point 1, see figure 3.4.

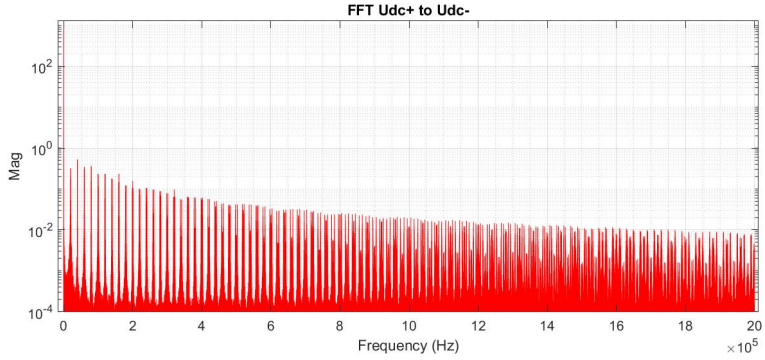


Figure 4.18: FFT calculation of Udc+ to Udc- up to 2MHz. The sampling time was 25ns and a total of 1.6M samples were used. The circuit is tuned. Measuring point 1, see figure 3.4.

Udc+ to ground

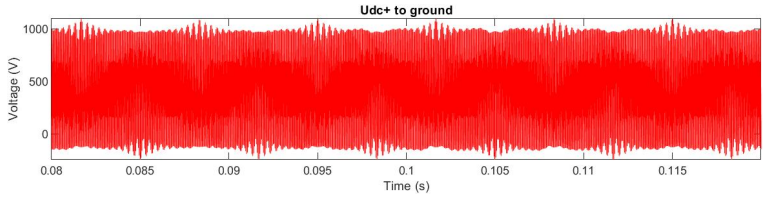


Figure 4.19: Udc+ to ground, over a time period of 40ms. The circuit is tuned. Measuring point 2, see figure 3.4.

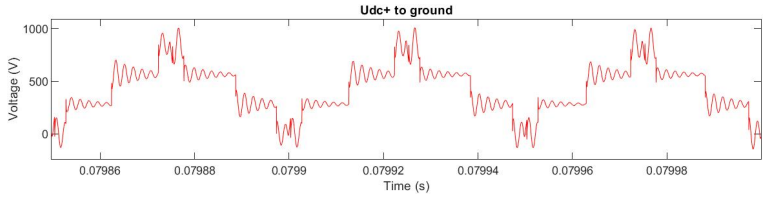


Figure 4.20: Udc+ to ground, plotted for a time window corresponding to 3 modulation periods (150µs). The circuit is tuned. Measuring point 2, see figure 3.4.

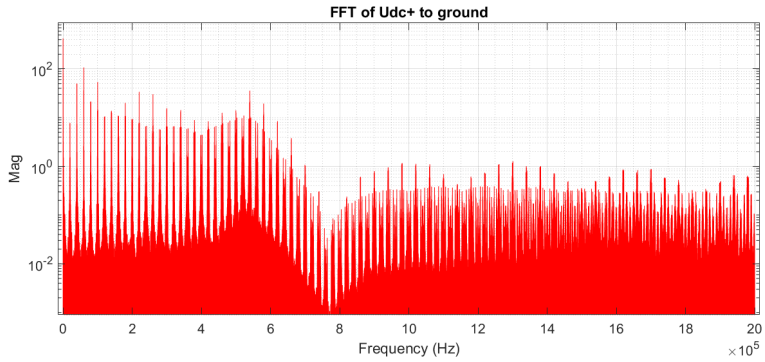


Figure 4.21: FFT calculation of Udc+ to ground up to 2MHz. The sampling time was $25ns$ and a total of 1.6M samples were used. The circuit is tuned. Measuring point 2, see figure 3.4.

AC output voltage

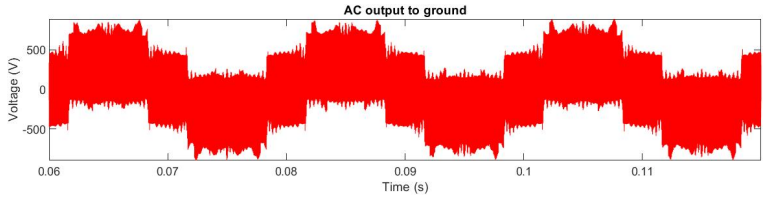


Figure 4.22: Voltage of AC output to ground. Simulated for 60ms. The circuit is tuned. Measuring point 3, see figure 3.4.

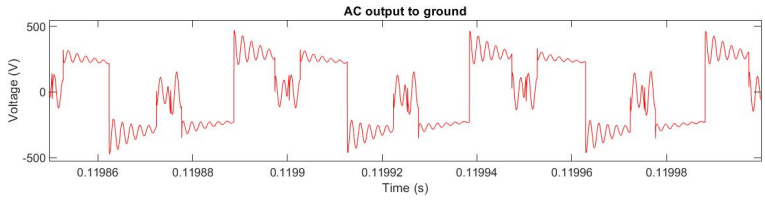


Figure 4.23: Voltage of AC output to ground in time domain, plotted for a time window corresponding to 3 modulation periods (150µs). Zoomed at the end of figure 4.22. The circuit is tuned. Measuring point 3, see figure 3.4.

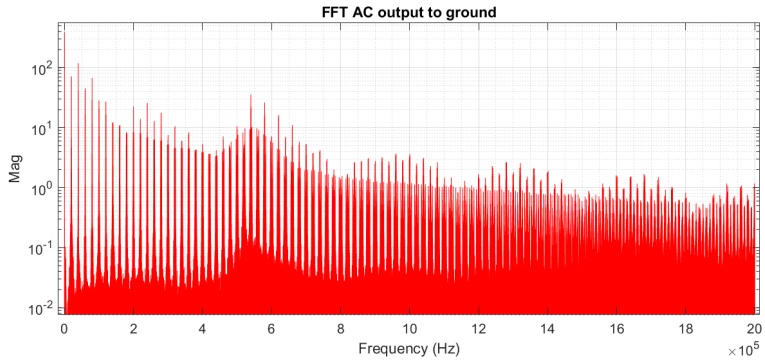


Figure 4.24: FFT calculation of AC output voltage up to 2MHz. The sampling time was 25ns and a total of 2.4M samples were used. The circuit is tuned. Measuring point 3, see figure 3.4.

L1 current

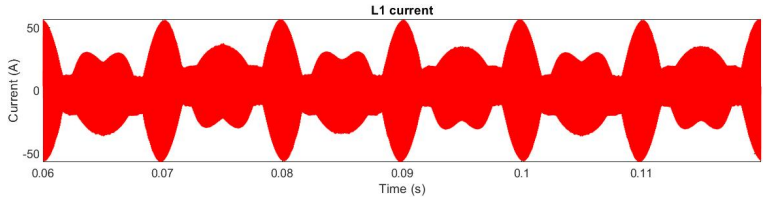


Figure 4.25: L1 current in the time domain, simulated for 60ms. The circuit is tuned. Measuring point 4, see figure 3.4.

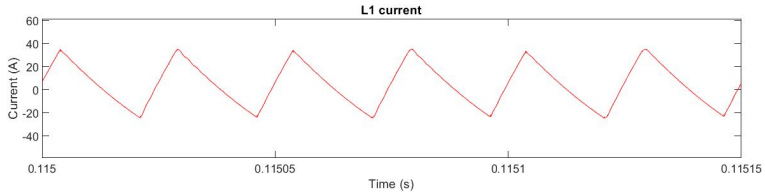


Figure 4.26: L1 current plotted for a time window corresponding to 3 modulation periods (150µs). The circuit is tuned. Measuring point 3, see figure 3.4.

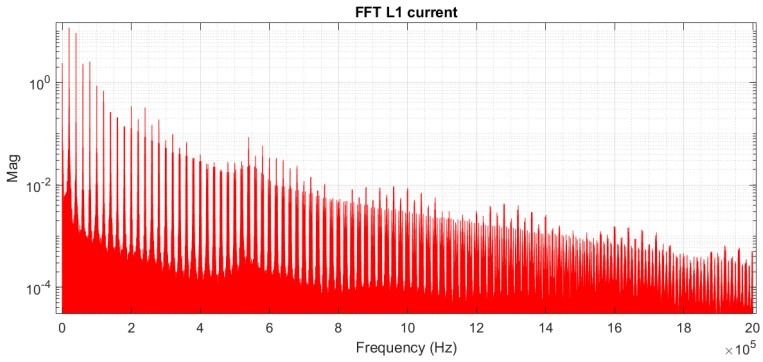


Figure 4.27: FFT calculation of L1 current up to 2MHz. The sampling time was $25ns$ and a total of 2.4M samples were used. The circuit is tuned. Measuring point 3, see figure 3.4.

4.2.3 Analysis of the result

The tuning has adjusted the frequency difference in the UDC+ to ground signals as well as increased the damping in the simulations to mimic the measured damping. In the FFT, the peak has been shifted slightly to higher frequency, see figure 4.21. Comparing figures 3.9 and 4.20 large similarities are present in UDC+ to ground voltages. The dissimilarities and their origins are discussed in chapter 5, especially the large damping resistor needed to get similar damping of the oscillations.

4.3 Common mode

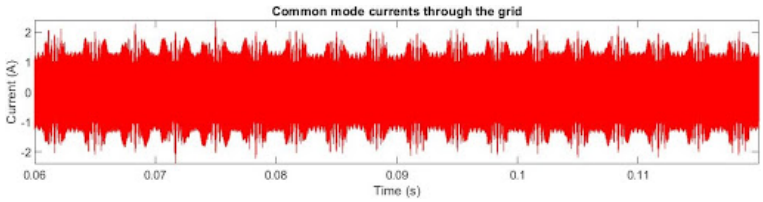


Figure 4.28: Common mode currents through the grid, in the time domain. Simulated for 60ms. The circuit is tuned. The current represents the sum of the currents flowing through parasites to ground.

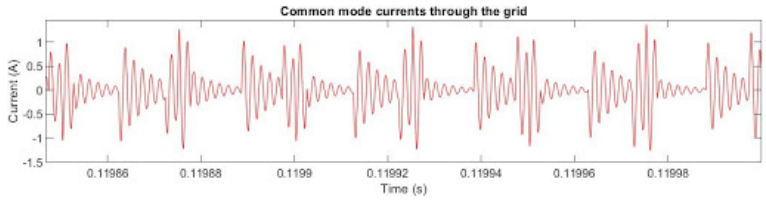


Figure 4.29: Common mode currents through the grid. Plotted for a time window corresponding to 3 modulation periods. The circuit is tuned. The current represents the sum of the currents flowing through parasites to ground.

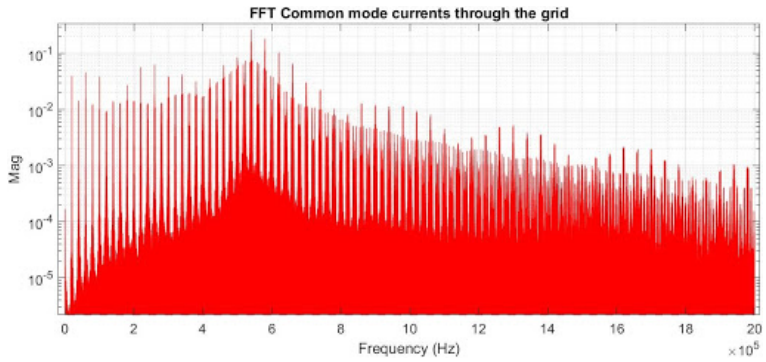


Figure 4.30: FFT calculation of the common mode current up to 2MHz. The sampling time was $25ns$ and a total of 2.4M samples were used. The circuit is tuned. The current represents the sum of the currents flowing through parasites to ground.

When simulating the CM currents the amplitude is between 1A and 2A. Frequency wise the simulated signal contains a 540kHz oscillation. A closer comparison between the measured and simulated common mode currents is done in chapter 5.

Chapter 5

Discussion

5.1 Simulation results using measured values

Viewing the simulations without tuning and comparing them to the measured signals from the DUT, possible errors in the parasitic element values can be analyzed. The frequency of 480kHz in the oscillations of the "UDC+ to ground" (figure 4.8) was a welcome match with the measured 540kHz (figure 3.10), even though it still differed slightly. As the main parameters of the measured inductances and capacitances are the cause for these oscillations, the measurement of components and parasites seems to be reasonably accurate. The same 480kHz oscillations show up in the AC output simulation (figure 4.11) as well because they are believed to be energy flowing between the line filter inductor, L1, and the parasitic capacitances in the converter. However in the measurement, the AC output oscillation is 740kHz (figure 3.13). The oscillations of 480kHz can be recognized in the simulation of L1 (figure 4.14) but not in the measured current of L1 (figure 3.16), this might be the result of a bandwidth limit of 100kHz in the current clamp.

Measuring error and component tolerance
The reason behind why the values from such a precise impedance analyzer still needed tuning might be variations in manufacturing accuracy between two components who share the same nominal value. Capacitors are for example rated in tolerance around the nominal capacitance. Some ratings allow an as high deviation as 20% from the nominal value [9]. If we assume a deviation of 5% in the inductor L1 the maximum difference in actual inductance between two inductors could be about 10%. If the measured inductor value was higher than its equivalent in the operating machine the difference might shift the resonant frequency 26kHz using equation 2.5.

$$26kHz = \frac{1}{(2 * \pi * \sqrt{1.1 * L1 * C_{par}})} - \frac{1}{(2 * \pi * \sqrt{0.9 * L1 * C_{par}})} \tag{5.1}$$

When measuring the components, cable lengths and cable loops should re-

semble the installed components as much as possible. Due to space optimization in the DUT, accessibility to the installed components has suffered. This makes it difficult to measure the components in their true surroundings and not doing so might affect the measurements. The cables are of course also home to parasitic elements and when measuring very small impedances, like parasites to ground, these "cable-parasites" might make up a considerable amount of the measured quantities. By making the cables as short as possible they can be minimized but for practical reasons this is more difficult than it might seem.

5.2 Simulation results using calibrated values

Tuning
After tuning the parameters, the frequency of the simulated Udc+ to ground oscillations (figure 4.21) are matching the 540kHz measured oscillations (figure 3.10). In addition, the damping coefficient of 0.69 is present in both simulated and measured oscillations. However, the tuning only affects parasites that are measured and found. No amount of tuning can therefore evoke another resonating circuit that might be present in the DUT. Therefore a proper investigation of where parasitic couplings are present is important. Missing components can not be tuned into place retroactively. To add more resonating circuits and higher frequency behavior, higher order equivalent circuits can be used, observe figure 2.10 in chapter 2. These would instead of introducing a single resonant frequency introduce multiple that could increase the high frequency accuracy of the model. Parameters at these frequencies are minute and a lot of care has to be put into the measuring-setup to measure their true value.

Resistive tuning
The fact that large adjustments are needed to make the damping coefficients to match is worth discussing. The resistor needed to increase the damping to an adequate level was 100-1000 times larger than the parasitic resistance measured from UDC to ground. A measurement error is therefore not probable. A component of this size "missing" probably means that there is an impedance in the circuit that has not been included in the model. Resistance is present in every conducting material as mentioned in chapter 2. When measuring a real world signal and comparing that to a simulation, where idealities are used, some differences are bound to show up. The needed resistor is however of considerable size indicating that there is something passing unnoticed. The solution to the damping problem in this thesis was including the large resistor when simulating but it is not plausible that such a resistor exists in the real world. The DUT is encapsuled by a metal chassi whose DC resistance does not come close to the needed 70Ω.

One way of explaining the resistance is taking into account the frequency of the currents flowing through the chassi and discussing eddy current power losses in the chassi. When high frequency currents flow through a conductor they will produce eddy currents, i.e. currents flowing normal to the main current. The

eddy currents generate resistive losses and could act as a part of the 70Ω resistor needed to achieve the correct damping. The amount of power loss depends on the geometry of the cross-sectional area in the conductor [7].

Another way high frequency currents flowing through the chassi could seem to be damped by a resistor is due to the skin effect. A high frequency current flowing through a conductor will, because of eddy currents, be distributed such that the current density is largest at the surface of the conductor. As frequencies increase the area transporting current decreases. Resistance through a conductor is inversely proportional to the area meaning the resistance could be larger than expected at a frequency like 540kHz [7].

Modeling such losses that are frequency dependent is not as straightforward as to include a single component in the model. To produce different effective impedance for different frequencies a capacitive, inductive ladder can be used. Different frequencies will pass through the different steps in the ladder and thus create a frequency dependent power loss [15].

IGBTs and model error
The simulated IGBTs have infinitely fast switching times meaning that they produce an excessive amount of harmonics compared to a real IGBT. Attempts of simulating a non-ideal IGBT have been made without success. This means that the model will always contain harmonics of higher values than the measured signal. However, this is useful when trying to find the upper limits of the electromagnetic emissions.

The drops/jumps that appear at the peaks of UDC+ to ground, shown in 4.1, are another cause of concern. These muddle the water, and make the comparison between simulation and measured signal harder to make. They will also affect the harmonic content of the simulated signal.

An interesting observation that establishes that the IGBTs are the driving components creating harmonic content, is the fact that the FFT of Udc+ to ground 4.21 consists of switching frequency multiples. The highest and most energy rich harmonics are caused by the switching. This again connects to the earlier statement about using ideal IGBTs in the simulation which might have a considerable effect on the frequency content.

5.3 Common mode currents

By viewing the currents flowing through the parasitic elements to ground in the simulation model, common mode currents can be analysed. Currents circling in the AF and currents flowing into the grid and returning through the grid currents can be simulated. Circling currents in the AF use one parasite to escape the AF and another to couple back into the machine. Both circling and escaping currents are of concern. Escaping currents will disturb other devices connected to the grid while internal common mode currents might interfere with the function of the AF. In the simulations no circling currents are present and all CM currents flow out into the grid.

Due to the current clamp's bandwidth limit of 100kHz, some distortion is bound to affect the signal at these frequencies. In the datasheet of Prosys CP- 35, the phase shift seems to decrease with about 5 degrees per decade at 100kHz, reaching a gain of -3dB at a phase shift of 45 degrees. This makes a measurement at 540kHz usable. Knowing this is however important when analysing the results [13].

When analysing the simulated common mode currents it is clear that the oscillations seen in UDC+ to ground are passing through the parasites to the chassi and onward through ground. In the measurements on the DUT similar oscillations are present. These also match the 540kHz oscillations seen in the tuned UDC+ to ground simulation. On a larger scale the amplitudes of the CM currents seem to lie between 1 and 2 amperes, see figure 5.1. The CM current amplitude is strongly coupled to the size of the parasitic elements connecting the DUTs internal parts to ground. The fact that these are similar indicates that the sizes of the parasites found are believable.

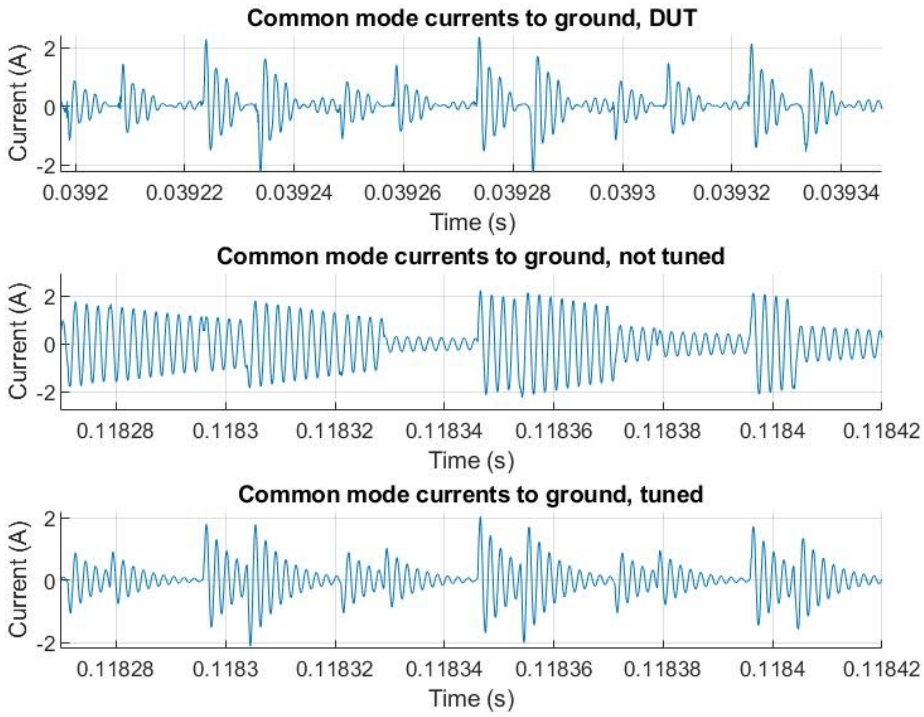


Figure 5.1: Common mode currents. Top measured on the DUT, Mid simulation with untuned model, Bottom tuned simulation.

Comparing the current in the simulation to its measured equivalent it is likely

that the oscillations originate from the same place in the model and in the DUT respectively. The tuned simulation matches the damping of the measured for the first three periods. Thereafter a non-linear damping of the measured takes place which differs from the simulated, again shown in figure 5.1.

5.4 Comparison

Small differences between the simulated and the measured signals can be found, both in time and frequency domain, but from a broader perspective the shapes and magnitudes are similar.

UDC+-

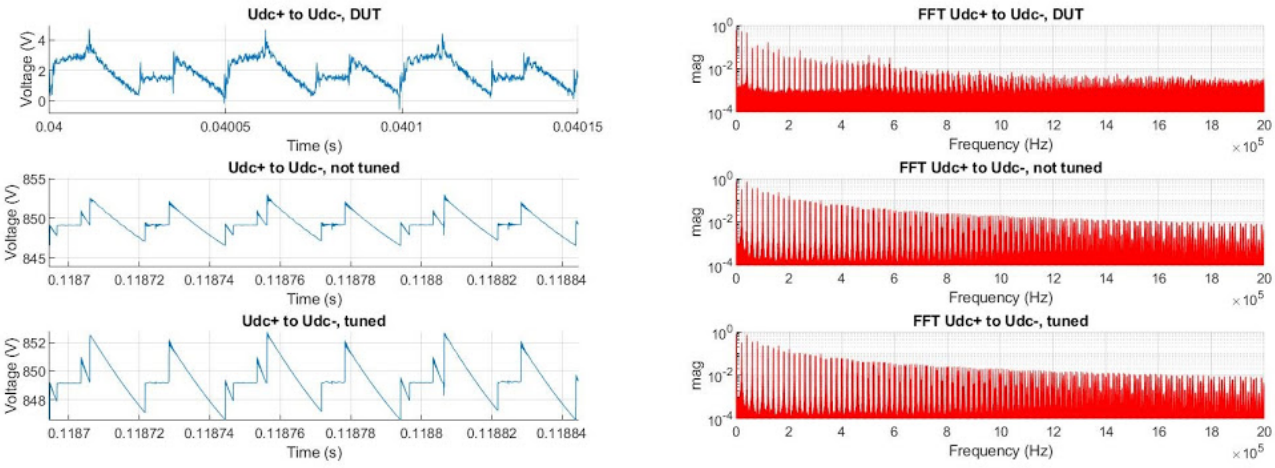


Figure 5.2: The voltage over the DC-link capacitor.

In figure 5.2 there is not much of a difference between the tuned model and the not tuned model. Except, there are small oscillations found in the model that is not tuned. The measured model appears thicker and slower due to its oscillations, however similar peaks appear in both measured and simulated signals.

UDC+ to ground

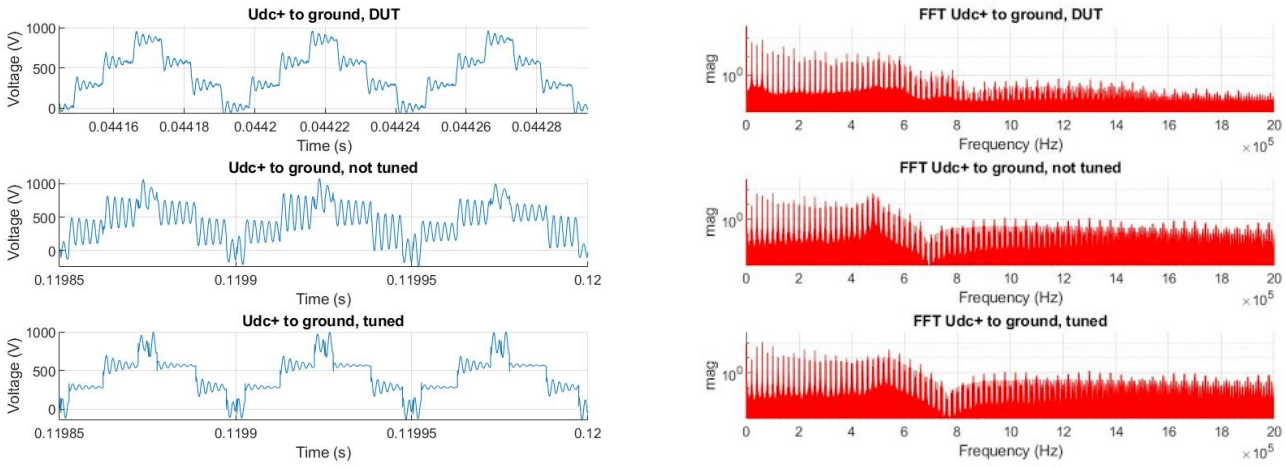


Figure 5.3: UDC+ to ground comparison.

UDC+ to ground is one of the more important signals to compare, which can be seen in figure 5.3 . The oscillations that show up in several measurements originate from here as the IGBTs switching directly affects the signal. The discussed oscillations are clearly visible in the measured and both simulations. The tuning effects are also clear as the damping has increased. The frequency was also increased slightly but this is more noticeable in the FFT comparison. In the time domain some differences are still present. Oscillation amplitude varies slightly in the simulation over the periods while they are constant in the measured signal. Comparing the FFTs, the 540kHz harmonic is present more clearly in the simulations compared to the measured signal. The measured signal still has a peak at 540kHz but the energy is more distributed over neighbouring frequencies as well. The signal, in time domain, seems quite clean and one might expect a cleaner FFT. The fact that the signals are mainly composed of square waves, very rich in harmonics, explains why the FFT is not clean and contains a lot of other frequencies.

AC Voltage output

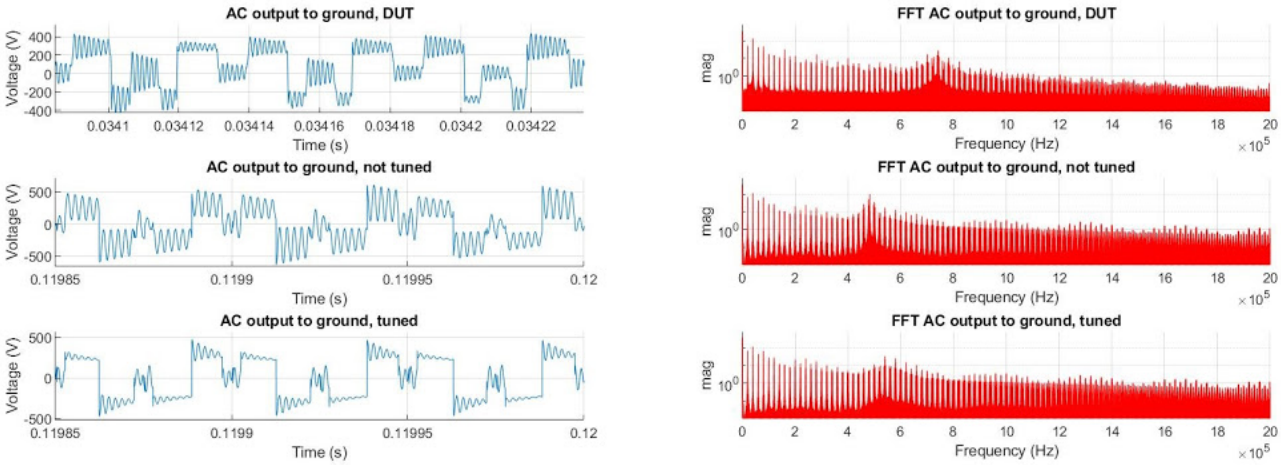


Figure 5.4: Ac output to ground comparison.

In figure 5.4 the square waves have a similar appearance, but the damping in the tuned model is too large. The model that is not tuned looks more similar to the measured signal with its more continuous oscillation. In the FFT comparison, a peak can clearly be recognized at 740kHz for the measured signal on the DUT, which is the oscillation on the "square wave". This peak is found at 480kHz for the model that is not tuned, and 540kHz in the tuned model. These are the same frequency peaks found in Udc+ to ground simulations. The tuned model is off with 200kHz. This implies that there are different components causing this oscillation compared to the ones in UDC+ to ground. The AC terminals on the IGBTs have their own parasites and another oscillation could appear between these specific parasites and L1 in the LCL filter. It should be noticed that the frequency in the simulations are of the same frequency as the simulated UDC+ to ground oscillations. But this is not the case in the measured signals. A higher frequency oscillation in the measured signal means, using equation 2.5, that a smaller L*C is active. The wavy appearance in the FFT comparison is worth noting. Above 800kHz the harmonic content created by a trapezoid can be recognized from figure 2.12.

5.5 Measurement uncertainty

There are various measurement uncertainties that can be found in the lab setup. Random uncertainties of the lab setup can occur from the environment through EMI. These interferences will be picked up in the measuring equipment, but the average error will be zero. The DUT was measured without an added load to the system, however, there could exist unknown loads in the system that the DUT recognizes. Systematic uncertainties can be found when measuring currents and voltages, it is crucial that the equipment have enough bandwidth for the purpose. The differential USB oscilloscope "Picoscope 4444" sampled at 16Ms/s and the voltage probe Tektronix p5200a had a bandwidth of 50MHz. The bottleneck in this case was the Picoscope 4444, and using Nyquist criterion the measurement is adequate for frequencies up to 8MHz (16/2 Ms/s). The bandwidth of the current clamp "GMC-I Prosys CP- 35" is 100kHz which gives results that are damped at higher frequencies. When using the Hp 4194A impedance analyser, the cables should be as short as possible to minimise parasitics, but there will be some constant error through all measurements. Illegitimate error can be faulty circuits in the measuring equipment, or wrong use of equipment. The current clamp "GMC-I Prosys CP- 35" with a bandwidth of 100kHz can be classified as this type of error if used at higher frequencies [4].

Chapter 6

Conclusion

6.1 Concluding thoughts

The developed simulation model is suitable for simulating high frequency behavior in an active filter. The model can however not be viewed as the entire truth but can act as a foundation in increasing the high frequency understanding. With this in mind modeling and analysing high frequency behavior is absolutely possible.

The model can be used without tuning as a component- and parasitic schematic of the DUT, where measured impedances are measured up to 10MHz. The model can also be used with tuning as a test program that simulates the DUT and some high frequency behavior. The model can be made more detailed to get a better accuracy at higher frequencies. Nevertheless, it will be difficult and more accurate equipment is needed to improve already measured impedances. Further, the adjusted model can simulate a common mode current that is verified up to 100kHz. However, a common mode current can be approximated including frequencies reaching 540kHz. An exact frequency limit where the model is no longer viable is difficult to draw as there are winnings to be had even when simulation and reality differs. The goal of building a 1MHz model was in some sense accomplished while work still remains to truly model the DUT correctly.

6.2 Future work

6.2.1 Model improvements

One way to improve upon the model and increase the believability of it is measuring the parasitic elements as the components are installed in the DUT. As mentioned previously this is difficult but doing so would give a better understanding of how the parasitic couplings work. Another way, that is strictly a model improvement, is to model the IGBTs as non-ideal components. The simulated IGBTs have infinitely fast switching times meaning that they produce

an excessive amount of harmonics compared to a real IGBT.

The resistive component that has not been pinpointed but is acting on the oscillations throughout the DUT is an important factor in improving the simulation model. Although the damping coefficient can be tuned to a better value, the model loses believability and this tuning might affect other parts of the model that also play a part in the harmonic footprint of the DUT. Implementing impedance ladders as discussed to model power losses in eddy currents and due to skin effect might yield interesting results.

An interesting way forward would also be to run the DUT in an active state where the AF is compensating for a load. Both active power harmonics and reactive power compensation would affect the operation of the AF and produce a different harmonic footprint. If the simulation under identical conditions still achieves a decent match, the model shows resilience. It means that the model is less likely to be an optimization of a single operation condition. This is important to know before the model is used as an instrument to analyze the DUT.

6.2.2 Common mode work

Common mode guidance

As the model becomes more believable, work can be performed to investigate the CM currents. More specifically, how to keep them from escaping into the grid where they affect other devices. One such strategy worth investigating is common mode current guidance. The working principle is creating a low impedance pathway for high frequency CM currents between the converter's DC side and the line filter capacitor. This might keep CM currents circling within the DUT instead of reaching the grid, thus reducing the conducted emissions from the DUT.

Interleaving

When common mode currents are understood in the model it can also be used to analyze the effectiveness of a method called interleaving. Interleaving is a method where multiple, N, AFs are connected in parallel and their PWM is shifted by $\frac{360^\circ}{N}$ from each other. By doing this, the N:th order harmonics will be canceled in theory. This is an interesting method when considering that using multiple modular AFs is common in larger AF installations. Interleaving would mostly reduce lower frequency content reaching 100kHz but high frequency content might also be affected [6].

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